

WHAT IS CLAIMED IS:

1. An information reproducing apparatus, which supplies a read signal reproduced from a recording medium to a maximum likelihood decoding means, and
5 decodes and reproduces a data, comprising:
 - a clock source for supplying a clock signal to the maximum likelihood decoding means;
 - clock control means interposed between the clock source and the maximum likelihood decoding means; and
- 10 a controller for controlling an operation mode such as decoding or the like,
the clock control means supplying the clock signal to the maximum likelihood decoding means in only decoding.
- 15 2. The information reproducing apparatus according to claim 1, wherein the maximum likelihood decoding means is a Viterbi decoder.
- 20 3. The information reproducing apparatus according to claim 2, wherein when the maximum likelihood decoding means is a Viterbi decoder, waveform equalization means for the read signal is provided on a pre-stage of the Viterbi decoder.
4. The information reproducing apparatus according to claim 3, wherein the waveform equalization characteristic is a partial response characteristic.
- 25 5. The information reproducing apparatus according to claim 4, wherein a PR (1, 2, 1) characteristic is used as the partial response characteristic PR.

6. The information reproducing apparatus according to claim 4, wherein a PR (1, 3, 3, 1) characteristic is used as the partial response characteristic PR.

5 7. The information reproducing apparatus according to claim 2, wherein the
Viterbi decoder is composed: of a branch metric circuit for calculating a branch metric
from a read signal; an adder-comparator-selector circuit for adding the branch metric
and a path metric, and selecting a transition state; a status memory block for holding a
selected status data; and a data merge block for decoding the read signal from the
10 status data.

8. The information reproducing apparatus according to claim 1, wherein the read signal is a signal from a magneto-optical disk.

9. The information reproducing apparatus according to claim 1, wherein the clock source is a PLL circuit to which the read signal is supplied.

10. The information reproducing apparatus according to claim 1, wherein the clock control means is composed of a clock driver, switching means provided on a pre-stage of the clock driver, and two logical product circuits provided on a pre-stage of the switching means, and

the clock signal is supplied in common to the two logical product circuits.

11. The information reproducing apparatus according to claim 10, wherein a
read gate signal obtained from the controller is supplied to a first logical product circuit

of first and second logical product circuits, and a control signal indicative of a power saving mode state and generated by the controller is supplied to the second logical product circuit and the switching means.

5

TOP SECRET • DECODED